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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,470	02/05/2004	Nobuyuki Ikezawa	081848-0190	2935

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EXAMINER	
LEE, CALVIN	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,470	IKEZAWA, NOBUYUKI	
	Examiner	Art Unit	
	Lee Calvin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

OFFICE ACTION

Drawings

1. Figures 6-8(A & B) should be designated by a legend such as --Prior Art-- because only those, which are old, are illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment.

Claim Rejections - 35 U.S.C. § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country more than one year prior to the application date for patent in the United States
(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-2, 5-6, and 8 are rejected under 35 U.S.C. 102(**b**) as anticipated by *Han*.

a) *Han (US 6,103,603)* discloses a method for forming a semiconductor device, comprising of -doping nMOS area with n-type dopants and pMOS area with p-type dopants [Figs. 3B and 3C] -selectively etching a first (upper) portion of a doped polysilicon film **33d** by using a first etching condition and a second (lower) portion of the doped polysilicon film by using a second etching condition to thereby form gate electrodes **33a** and **33b** from the first and second film portions [cols. 3-4.and Fig. 3D], wherein the first etching condition generating a less amount of side etching (i.e., gate with vertical sidewalls) compared to the second etching condition [col. 5, ln.38].

Although *Han* is silent about the polysilicon film's "first portion doped with impurities at a first impurity concentration and a second portion doped with impurities at a second impurity concentration which is lower than the first impurity concentration," it is understood from the semiconductor implantation processing art that the impurity polysilicon film in each of the MOS area has a higher impurity concentration at the top of the film compared to the lower impurity concentration at the film bottom due to the effect of an ion diffusion.

Therefore, *Han* inherently teaches or suggests a second impurity concentration of the doping film being lower than a first impurity concentration.

b) In re claims 5-6 and 8, *Han* suggests the first etching condition using CF_4 etching gas [col. 5, ln.5] and the second etching condition initially using a mixture of Cl_2 and HBr and subsequently a mixture of Cl_2, HBr, He, and 0_2 [col. 5, ln.10].

4. Claims 1, 3-4, and 8 are rejected under 35 U.S.C. 102(**b**) as anticipated by *Tao et al.*

Tao et al al (US 6,242,350) discloses a method for forming a semiconductor device:
-forming a polysilicon film **46** including a first portion doped with impurities at a first impurity concentration and a second portion doped with impurities at a second impurity concentration which is lower than the first impurity concentration [col. 3, ln.62]
-forming an organic anti-reflection film **52** before subsequent etching steps [col. 3, ln.64]
-and selectively etching a first (upper) portion of the doped polysilicon film by using a first etching condition and a second (lower) portion of the doped polysilicon film by using a second etching condition to thereby form a gate electrode from the first and second film portions [col. 4], wherein the first etching condition generating a less amount of side etching (i.e., gate with vertical sidewalls) compared to the second etching condition [col. 5, ln.38].

Tao et al also suggests the first and second etching conditions [col. 4, ln.50] using a mixture of Cl_2 and HBr in a carrier gas of Helium (meets the pending claim 8).

5. Claims 1, 5-6, and 8 are rejected under 35 U.S.C. 102(**e**) as anticipated by *Yoshida et al.*

a) *Yoshida et al (US 6,531,349)* discloses a method for forming a semiconductor device, comprising the step of selectively etching a first (upper) portion of a doped polysilicon film **12** by using a first etching condition [Fig. 3B] and a second (lower) portion of the doped polysilicon film by using a second etching condition [Fig. 3C] to thereby form a gate electrode from the first and second film portions, wherein the first etching condition generating a less amount of side etching (i.e., uniform the gate thickness) compared to the second etching condition [col. 2, ln.63].

Although *Yoshida et al* is silent about the polysilicon film's "first portion doped with impurities at a first impurity concentration and a second portion doped with impurities at a second impurity concentration which is lower than the first impurity concentration," it is understood from the semiconductor implantation processing art that the impurity polysilicon film in the MOS area has a higher impurity concentration at the top of the film compared to the lower impurity concentration at the film bottom due to the effect of an ion diffusion.

Therefore, *Yoshida et al* inherently teaches or suggests a second impurity concentration of the doping film being lower than a first impurity concentration.

b) In re claims 5-6 and 8, *Yoshida et al* discloses the first etching condition using a mixture of Cl_2, HBr, and CF_4 etching gas [col. 2, ln.53] and the second etching condition using HBr and 0_2.

Allowable Subject Matter

6. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Yoshida et al suggests the first etching condition includes an ambient pressure of 5 to 15mTorr, a source power of 300 watts, a bias power of 60 watts. However, none of the cited arts including *Yoshida et al* suggests a volume ratio of the CF-based gas to total gas at 75 % or more.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: *Nallan et al (US 2004/0009634)* discloses a two-step etch process comprised of etching a first (upper) portion of a polysilicon film **106** by using one or several chlorinated/brominated /fluorinated chemistries (e.g., Cl_2, HBr, and CF_4 and the like) [pg. 1] and a second (lower) portion of the polysilicon film by using a mixture of HBr/Cl_2 etchant with N_2 gas to thereby form a gate.

8. Any inquiry concerning this communication from the Examiner should be directed to *Calvin Lee* at (571) 272-1896 from 7:00 to 17:00 (Monday-Thursday, Eastern Time). If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2825's Supervisory Patent Examiner *Matthew Smith* can be reached at (571) 272-1907.

Any inquiry relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0596. The central fax number is (703) 872-9306 for all communications to be entered (e.g., amendments, remarks, IDS, etc.)

calvin lee

November 12, 2004